REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended claim 14 to recite that the plural semiconductor-mounting substrate portions are each for mounting a "respective" semiconductor device; to recite that a connecting portion is for connecting the plural semiconductor-mounting substrate portions; and to recite that "each of" the semiconductor-mounting substrate "portions" comprises specified wirings that include an external connection terminal a wire bonding terminal.

In addition, Applicants are adding new claims 24-26 to the application. Claim 24, dependent on claim 14, recites that the wire bonding terminal is a terminal for connecting a wire from the semiconductor device thereto. Claims 25 and 26, dependent respectively on claims 24 and 14, recite that the external connection terminal is for electrically connecting the substrate to an outer wiring. Note, e.g., Fig. 1f and the description bridging pages 19 and 20 of Applicants' specification.

Applicants respectfully traverse the rejection of their claims as set forth in the Office Action mailed February 8, 2005, particularly insofar as this rejection is applicable to the presently amended claims, and respectfully submit that all of the presently pending claims patentably distinguish over the teachings of the applied reference, that is, the teachings U.S. Patent No. 5,381,039 to Morrison, under the requirements of 35 U.S.C 102 and 35 U.S.C 103.

It is respectfully submitted that this reference as applied by the Examiner would have neither taught nor would have suggested such a substrate for mounting a semiconductor device as in the present claims, including, inter alia, wherein the substrate has plural semiconductor-mounting portions, each for mounting a respective semiconductor device, with a connecting portion for connecting the plural semiconductor-mounting substrate portions, and a registration mark portion, and wherein each of the semiconductor-mounting substrate portions includes wirings that include an external connection terminal and a specified wire bonding terminal positioned specifically relative to each other, with the connecting portion including an electrically conductive layer. See claim 1.

As is clear from Applicants' disclosure, through use of the substrate as recited in the present claims, including wherein the connecting portion includes an electrically conductive layer, a sufficiently rigid substrate for mounting a plurality of semiconductor devices thereon (which, for example, can later be separated into individual packaged devices), is achieved. In addition, through use of the wirings including the external connection terminal and wire bonding terminal positioned as in the present claims, a relatively small device can be achieved, as compared with, e.g., a device having leads extending outwards of the semiconductor device. Furthermore, through the use of the registration mark portion, the substrate can easily and effectively be positioned for, e.g., mounting and subsequently separating packaged semiconductor devices.

In particular, according to the present invention, wherein the wire bonding terminal is a terminal for connecting a wire from the semiconductor

device to such wire bonding terminal, and especially wherein the external connection terminal is for electrically connecting the substrate to an outer wiring, with the external connection terminal and wiring bonding terminal provided as set forth the present claims, a very compact device which can achieved, for example, a chip scale package can be obtained.

Morrison discloses a semiconductor device, more specifically a hermetic semiconductor device having jumper leads, more particularly a device having a ceramic base with a plurality of conductive pads or jumper leads on a surface thereof. The patent discloses that a lead frame having a plurality of conductors is attached to a periphery of the ceramic base with a glass material; and a semiconductor die is bonded and directly electrically connected to the surface of the ceramic base, the plurality of conductors of the lead frame being wire bonded to the plurality of conductive pads of the ceramic base to electrically connect the semiconductor die to the lead frame. Note, in particular, column 2, lines 18-29, of Morrison. As applied by the Examiner, and noting, for example, Fig. 2 of this patent this patent discloses a hermetic semiconductor device 40 (see Fig. 2) which combines with a flip-chip attachment method with a cerquad design to provide hermetic packaging for semiconductor dice having array bonding pads. A multi-layer ceramic base 42 has a first array of conductive pads 44 on an inner surface, the first array being used to form physical and electrical connections with semiconductor die 46. An array of conductive pads 28 on the inner surface of the multi-layer ceramic base 42 is electrically interconnected to the first array of conductive pads 44, and a plurality of wire bonds 20 are formed between the plurality of conductors of the lead frame 16 and the second array of conductive pads 28

to establish electrical connections between the multi-layer base 42 and the lead frame 16. Note from column 4, line 60 through column 5, lines 30, of Morrison.

As can be seen in Morrison, the wire bonding terminal constitutes an external connection terminal, with the conductive pads 44 forming electrical connection to the semiconductor die 46. It is respectfully submitted that this disclosure of Morrison would have neither taught nor would have suggested, and in fact would have taught away from, structure as in the present claims, including wherein each of the semiconductor-mounting substrate portions includes wirings that include an external connection terminal and a wire bonding terminal provided in an outer side of said external connection terminal.

Furthermore, as applied by the Examiner, a plurality of connecting portions are used which the Examiner contends connects the plural substrates 44. As is clear from the teachings of Morrison, 44 therein refers to a first array of conductive pads. It is respectfully submitted that such disclosure in Morrison would have neither taught nor would have suggested the connecting portions for connecting the plural semiconductor-mounting substrate portions, each for mounting a respective semiconductor device, as in the present claims, and advantages thereof, for example, for effectively and efficiently mounting a plurality of semiconductor devices.

Furthermore, the Examiner has generally referred to Fig. 2 as showing a registration mark portion. Contrary to this allegation by the Examiner, it is respectfully submitted that Morrison does not disclose, nor would have suggested, such a registration mark portion as in the present claims. In this

regard, if the Examiner maintains the prior art rejection, the Examiner is respectfully requested to point out the specific portion of Fig. 2 of Morrison (e.g. through a description in the specification thereof) showing a registration mark portion.

It is further noted that the Examiner points to wires 20 as being a connecting portion that comprises an electrically conductive layer. However, note that in the present claims, the connecting portions, which comprise an electrically conductive layer, is for connecting the plural semiconductor-mounting substrate portions. It is respectfully that Morrison would have neither taught nor would have suggested such connecting portion, much less that such connecting portion comprises an electrically conductive layer, as in the present claims, and advantages thereof.

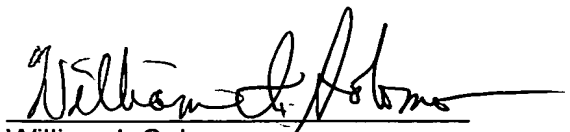
Furthermore, note the more specific recitation in connection with the wire bonding terminal and external connection terminal, as in various of the present claims. Clearly, Morrison would have neither taught nor would have suggested the wire bonding and external connection terminal as further defined in claims 24-26, and advantages thereof in, e.g., providing a smaller device, e.g., a chip scale package.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims remaining in the application are respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to

Deposit Account No. 01-2135 (Case No. 566.43481VC5) and please credit any excess fees to such deposit account.

Respectfully submitted,



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Attachments